ANALYTICAL MODEL OF NOISE IN AN ANALOG FREQUENCY DIVIDER

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ABSTRACT

The noise properties of a microwave analog frequency divider are investigated. The division is realized with a field effect transistor in a forced oscillation mode. An appropriate model is proposed for the calculation of the output signal phase and amplitude noises from the input signal phase noise and from the transistor low frequency noise data.

INTRODUCTION

Analog frequency dividers have become essential circuits for FM communications and have been recently widely studied [1,2,3,4,5]. However the noise behaviour of these circuits is not so well known. Phase noise investigations on the Miller's regenerative divider [6] have already been presented [5]. Nevertheless, there is a need for a model able to predict the noise behaviour of a divider in which the mixing and amplifying functions are simultaneously realized by the same microwave transistor [1,7]. In that case, the transistor is in forced oscillation mode, harmonically controlled by the input signal [1].

Noise in synchronised oscillators has already been studied by Kurokawa [8]. However, Kurokawa's approach is limited to a small signal injection locking and low frequency noise conversion is not included in his analysis. Siweris and Schiek [9] have investigated noise up-conversion in free running oscillators using the conversion matrices formalism [10]. We use the same method in this paper. More closely related to our work, the paper of X. Zhang et al. [11] deals with the subharmonic injection locking of microwave oscillators. However, only a single nonlinearity is used in their work to analyse the locked oscillation mode. As it will be shown in this paper, reactive nonlinearities can be essential to describe the noise conversion process in harmonically synchronised oscillators, as in free running oscillators [9].

CIRCUIT DESCRIPTION

Figure 1 represents the frequency divider topology. In our case, the nonlinear active device N(er) is a field effect transistor biased in the pinch-off region to avoid free oscillations. The divider starts to operate when the FET is self-biased by the input signal. The self-biasing and the power characteristics of the divider can be well described using a model of the FET with one nonlinearity [1]. Similarly, the aim of our investigations on noise is to describe the divider noise behaviour using a simple FET model. However, the key element of noise conversion in a free running oscillator is the gate nonlinear capacitance [9]. It is therefore necessary to take into account this nonlinearity to evaluate the effect of the transistor low frequency (LF) noise on the output phase noise.

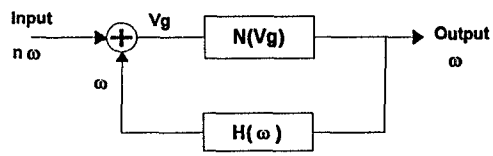

Figure 1 : *Frequency divider block diagram*

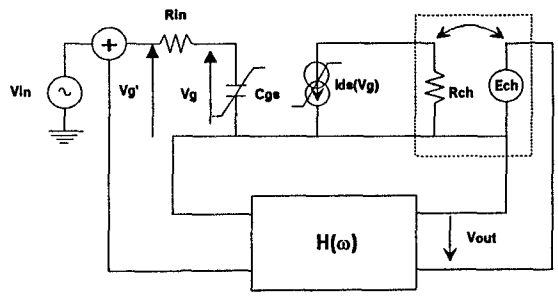

Figure 2 : *Circuit model of the divider*

The circuit representation of the divider is depicted in Figure 2. Third order polynomial expressions have been used to describe Ids(Vg) and Cgs(Vg). Moreover, the evolution of Cgs and Ids are limited to a gate voltage range [Vt,Vbi] where Vt is the pinch-off voltage and Vbi is the gate barrier built-in voltage.

Different feedback configurations have been investigated. Voltage feedback is considered in Figure 2.

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The load impedance Rch coupled to a voltage generator Ech stands for the isolator used in the experimental set-up. Rin represents the sum of the input load impedance (50Ω) and the input parasitic series resistances of the transistor. An alternative representation does not involve any isolator : therefore both current and voltage participate in the feedback. In this case, Rin is made of the parasitic resistances of the transistor plus the output charge impedance which is brought back to the input through the feedback circuit. The value of Rin is essential since the phase fluctuation results not only from the nonlinear Cgs but also from the nonlinear current created by Cgs across Rin. Actually no critical difference between the two models has been observed in the results and only the first model will be concerned in this paper since it seems to corresponds better with the measurement configuration.

CIRCUIT ANALYSIS

a) Feedback large signal condition :

Before analysing the noise conversion mechanism, it is necessary to know precisely the large signal value of the control voltage Vg. As an example, the loop condition can be written as :

$$H(\omega)\,R_{ch}\;\; Ids(Vg) = Vg' = Vg + R_{in}\;\; Cgs(Vg)\frac{dVg}{dt}$$

H(ω) is the transfer function of a resonator centered on the output frequency ω, with a quality factor Q, and the other parameters being defined in Figure 2. This system can be solved at the frequency ω using the Fourier development of Ids(Vg) and Cgs(Vg). The control voltage Vg is only composed of the loop voltage at ω, of the input voltage at nω and of the DC bias Vg0.

b) Noise conversion description :

The noise sidebands are evaluated at five frequencies. For example, the noise spectral components of the output current Ids are : Ids_{lf} at Ω, Ids_{1l} and Ids_{1u} at ω - Ω and ω + Ω, Ids_{2l} and Ids_{2u} at nω - Ω and nω + Ω where Ω is the baseband frequency (Ω << ω). They are obtained from the input noise data using the conversion matrix $[g_m]$:

$$\begin{bmatrix} Ids_{lf} \\ Ids_{1l}^{*} \\ Ids_{1u} \\ Ids_{2l}^{*} \\ Ids_{2u} \end{bmatrix} = \begin{bmatrix} g_0 & g_1 & g_1^{*} & g_n & g_n^{*} \\ g_1^{*} & g_0 & g_2^{*} & g_{n-1} & g_{n+1}^{*} \\ g_1 & g_2 & g_0 & g_{n+1} & g_{n-1}^{*} \\ g_n^{*} & g_{n-1}^{*} & g_{n+1}^{*} & g_0 & g_{2n}^{*} \\ g_n & g_{n+1} & g_{n-1} & g_{2n} & g_0 \end{bmatrix} \begin{bmatrix} Vg_{lf} \\ Vg_{1l}^{*} \\ Vg_{1u} \\ Vg_{2l}^{*} \\ Vg_{2u} \end{bmatrix}$$

Similarly, Igs is given by :

$$[Igs] = [j\omega]\,[Cgs]\,[Vg]$$

where [Cgs] is the gate capacitance conversion matrix. The loop condition is then written as in a) :

$$[H(\omega)]\,R_{ch}\,[g_m]\,[Vg] = [Vg'] = ([1] + j\,R_{in}\,[Cgs]\,[\omega])\,[Vg]$$

These expressions use 5th order matrices. However, [H(ω)] is supposed to have non-zero coefficients only at the ω - Ω and ω + Ω frequencies :

$$H_u = \frac{H_0}{1+2jQ\frac{\Omega}{\omega}} \qquad H_l = \frac{H_0}{1-2jQ\frac{\Omega}{\omega}}$$

where H_0 is the resonator transfer function at ω.

Therefore, these equations lead to a second order linear system where the unknown parameters are Vg_{1l} and Vg_{1u}. The amplitude noise and the phase noise are then calculated from Vg_{1l} and Vg_{1u}.

RESULTS

Firstly, it is interesting to note that with a zero amplitude input signal and transistor biasing conditions allowing the free oscillation, the problem is strictly similar to the one of noise conversion in a free running oscillator. Therefore, the first step to check the validity of the method is to evaluate the noise conversion in a free running oscillator. Figure 3 represents the phase noise of such an oscillator calculated and measured for a MESFET featuring approximately an 1/f LF noise which has previously being fully characterized.

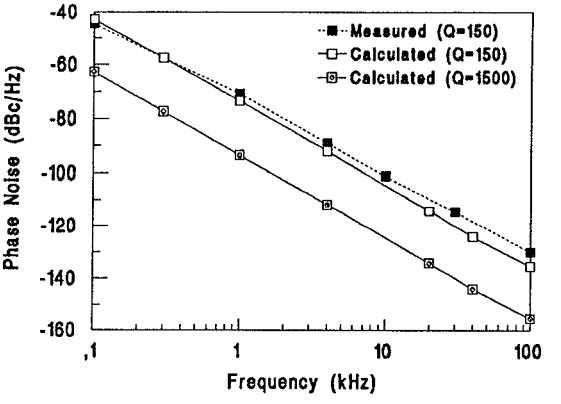

Figure 3 : *Phase noise of a 4 GHz MESFET free running oscillator versus the baseband frequency (Ω/2π).*

As it was expected, the slope of the phase noise is 30 dB/dec and the calculated phase noise is inversely proportional to the feedback resonator quality factor [12]. The agreement between calculated and measured values is better than 5 dB. These results were therefore encouraging enough to proceed with the simulation of a divider by two.

Figure 4 represents different measured phase noise spectra which illustrate the benefits of such a divider concerning the phase noise. Spectrum 1 corresponds to the phase noise of an HEMT free running oscillator at 5 GHz. The same transistor is now used in a divider by two fed by a 10 GHz good spectral purity signal (spectrum 2). The divider output signal features a phase noise corresponding to spectrum 3, ie improved by 6 dB compared to the input in spite of the very noisy HEMT device. This phenomenon, similar to the noise reduction observed in injection locked oscillators, can be satisfactorily predicted with our model. Moreover our model is able to determine the influence of the input signal amplitude on the output signal spectral purity.

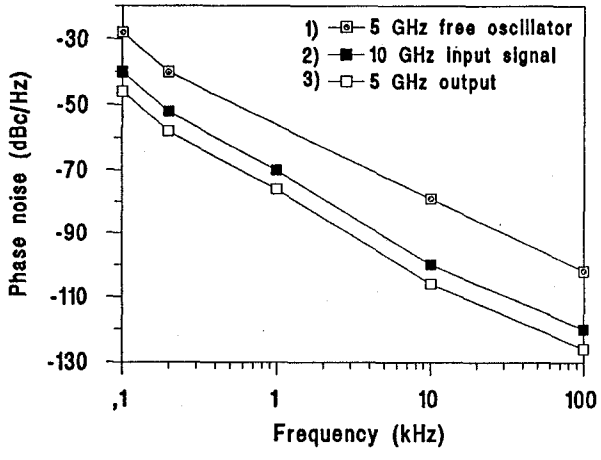

Figure 4 : *Measured input and output phase noise spectra of a divider by two (Pinput ~ 0 dBm) and noise of the divider in the free oscillator mode.*

Figure 5 represents the measured and the computed output signal phase noise (at 10 kHz off the carrier) versus input signal amplitude (more precisely the peak voltage of the 10 GHz component of the input control voltage Vg). For the largest amplitude values, the divider operates in the way previously described and the output phase noise is 6 dB less than the input one (-106 and -100 dBc/Hz resp.). For the smallest amplitude values (below -20 dBm) the divider stops to operate in a forced oscillation mode and the gate bias as to be slightly modified to obtain an harmonic injection locking mode. Our model is still valid to compute the phase noise data in such a mode of operation. As an example, theoretical calculation shows that if Cgs is arbitrarily kept constant the resulting predicted phase noise is very low. On the contrary, if the actual dependance of Cgs on Vg is considered an output signal phase noise of about -90 dBc/Hz is predicted. This value is somewhat lower than the measured one (-80 dBc/Hz) and such a discrepancy is mostly observed on HEMT devices. Further investigations are in progress.

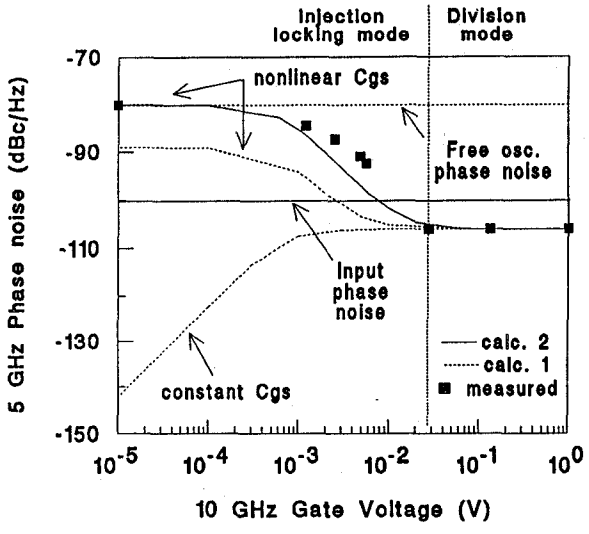

Figure 5 : *Frequency divider output phase noise at 10 kHz baseband frequency versus input signal voltage. Calculated 1 : phase noise is calculated from the input phase noise and from the measured LF noise of the transistor ; Calculated 2 : the LF noise is artificially increased to reach the measured phase noise of the free oscillator.*

Figure 6 and Figure 7 present the limits of the phase noise division versus two other parameters : LF noise spectral density and input phase noise. It was found that the noise division occurs for very high input LF noise or very low input phase noise. On Figure 7, the simulated phase noise is displayed for four different commercial FETs : one HEMT, two pseudomorphic HEMTs (PHEMT) and one MESFET. The differences that are observed in the output phase noise for very high input signal spectral purity result from differences in the LF noise and in the nonlinearity of each device. The other parameters that affect this level are : the input power (maintained at about 0 dBm) and the loop quality factor Q (equal to 150). For usual input signal noise levels and moderate Q any active device will provide similar output signal spectral purity. However, the use of a low LF noise transistor is recommended when one wants to use such a divider with very low noise input signals (< 140 dBc/Hz at 10 kHz and 0 dBm input). The MESFET [12] or the PHEMT [13] are then a better choice than classical HEMTs.

The amplitude noise only depends on the input LF noise of the transistor. This parameter could represent a problem for the low noise behaviour of the divider. It can be, in some cases, 20 dB higher than the phase noise limit (obtained when the input phase noise tends to zero) and the only way to minimizes it is to reduce the losses in the feedback loop.

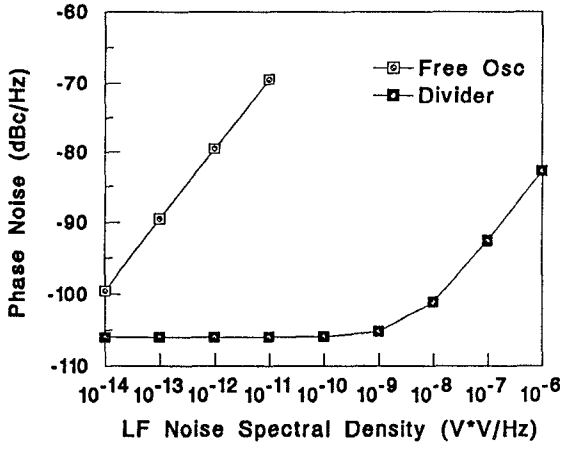

Figure 6 : *Phase Noise at 10 kHz off the 5 GHz carrier versus the LF input noise voltage spectral density (Input signal at 10 GHz : Pinput = 0 dBm)*

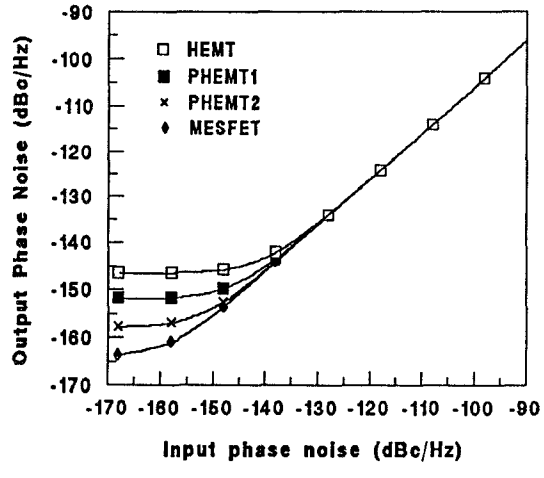

Figure 7 : *Simulated output phase noise at 5 GHz and 10 kHz baseband frequency versus 10 GHz input phase noise at 10 kHz baseband frequency for four different dividers realized with four different field effect transistors*

CONCLUSION

An analog X-band FET frequency divider has been modelled using two nonlinearities and the conversion matrices method. Good agreement has been found between measured and simulated data. The model has therefore been used to explain the phase noise division through the divider and to make clearer the working limits of such a circuit. We believe that present analysis could facilitate the design of low noise frequency dividers.

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